VERSION WITH MARKINGS TO SHOW CHANGES MADE

SPECIFICATION:

Specification at page 4, line 13:

~~The 1st invention~~ One aspect of the present invention is an asynchronous FIFO circuit comprising:

Specification at page 5, line 10:

~~The 2nd invention~~ Another aspect of the present invention is an asynchronous FIFO circuit comprising:

Specification at page 7, line 3:

~~The 3rd invention~~ Still another aspect of the present invention is the asynchronous FIFO circuit ~~according to 1st or 2nd inventions~~, wherein said error write counter and said error read counter are formed of a gray code counter.

Specification at page 7, line 7:

~~The 4th invention~~ Yet still another aspect of the present invention is an asynchronous FIFO data reading and writing method comprising:

Specification at page 8, line 1:

~~The 5th invention~~ Still yet another aspect of the present invention is an asynchronous FIFO data reading and writing method comprising:

Specification at page 9, line 20:

~~The 6th invention~~ A further aspect of the present invention is the asynchronous FIFO data reading and writing method ~~according to 4th or 5th inventions~~, wherein said error write step and said error read step are formed of a gray code count step.